

ABSTRACT

In a system having a received PN clock signal, a method is disclosed for providing a synchronized system clock signal having reduced jitter wherein the synchronized system clock signal is synchronized with the received PN clock signal. The method includes providing a stable high frequency reference signal and dividing the high frequency reference signal to provide a system clock signal having a plurality of system clock phases. The method also includes adjustably selecting a system clock phase of the plurality of system clock phases in accordance with the received PN signal in order to provide the synchronized system clock signal. The received PN clock signal is recovered by providing PN phase adjustments of the received PN clock signal. A tracking control signal is provided in accordance with the PN phase adjustments and the system clock phase is adjustably selected in accordance with the tracking control signal. The high frequency reference signal can be multiplied prior to the dividing.